GATE Computer Science Engineering Coaching by IGC

CO Assignment – 1

Q1. Consider the following register-transfer language

$$R_3 \leftarrow R_3 + M[R_1 + R_2]$$

Where $R_1$, $R_2$ are the CPU registers and M is a memory location in primary memory. Which addressing mode is suitable for above register-transfer language ?

a) Immediate
b) Indexed
c) direct
d) Displacement

Q2. In a 16 - bit instruction code format 3 bit operation code, 12 bit address and 1 bit is assigned for address mode designation. For indirect address, the mode bit is

a) 0
b) 1
c) Pointer
d) Off-set

Q3. Which set of instruction transfers the memory word specified by the effective address to AC or Load to AC ?

a) DR ← M[AR]
   AC ← AC + DR, E ← $C_{out}$, SC ← 0
b) DR ← M[AR]
   AC ← DR, SC ← 0
c) M[AR] ← AC, SC ← 0
d) DR ← M[AR]
   AC ← AC ^ DR, SC ← 0

Q4. The average memory access time for a machine with a cache hit rate of 90 % where the cache access time is 10 ns and the memory access time is 100 ns is

a) 55 ns
b) 45 ns
c) 90 ns
d) 19 ns

Q5. In a two level memory hierarchy, the access time of the cache memory is 12 nanoseconds and the access time of the main memory is 1.5 microseconds. The hit ratio is 0.98. What is the average access time of the two level memory system ?

a) 13.5 ns
b) 42 ns
c) 7.56 ns
d) 41.76 ns

Q6. Consider the following organisation of main memory and cache memory.
Main memory: 64K X 16
Cache memory: 256 X 16
Memory is word-addressable and block size is of 8 words. Determine the size of tag field if direct mapping is used for transforming data from main memory to cache memory.

a) 5 bits
b) 6 bits
c) 7 bits
d) 8 bits

Q7. A computer system has 4K-word cache organized in a block-set-associative manner, with 4 blocks per set, 64 words per block. Memory is word addressable. The number of bits in the SET and WORD fields of the main memory address format is

a) 15, 4
b) 6, 4
c) 7, 6
d) 4, 6

Q8 and Q9 are linked.

Q8. If the memory clip size is 256 X 1 bits, then how many clips are required to make up 1KB of memory ?

a) 8
b) 16
c) 24
d) 32

Q9. Considering the number of clips as base, find decimal form of 50.

a) 40
b) 80
c) 120
d) 160

Q10. A CPU has an arithmetic unit that adds bytes and then sets its V,C and Z flag bits as follows. The V-bit is set if arithmetic overflow occurs (in 2's complement arithmetic). The C-bit is set if a carry-out is generated from the most significant bit during an operation. The Z-bit is set if the result is zero. What are the values of the V, C and Z flag bit after 8-bit 1100 1100 and 1000 1111 are added ?

| | V | C | Z |
|---|---|---|---|
| a) | 0 | 0 | 0 |
| b) | 1 | 1 | 0 |
| c) | 1 | 1 | 1 |
| d) | 0 | 1 | 0 |

Q11. Consider the following sequence of instructions intended for execution on a stack machine. Each arithmetic operation pops the second operand, operates on them, and then pushes the result back onto the stack.

```
Push  b
Push  x
Add
Pop   c
Push  c
Push  y
Add
Push  c
Sub
Pop   z
```

Which of the following statements is/are true ?

1. If push and pop instructions each require 5 bytes of storage, and arithmetic operations each require 1 byte of storage then the instruction sequence as a whole requires a total of 40 bytes of storage.
2. At the end of execution, z contains the same value as y.
3. At the end of execution, the stack is empty.

a) 1 only
b) 2 only
c) 2 and 3 only
d) 1 and 3 only

Q12. A certain computer system design has a single CPU, a two-level cache, and supports memory mapped I/O for output-only controllers. Which of the following is true ?

a) The design is impossible, since memory mapped I/O will prevent cache coherence.
b) In two-level caches, the $L_1$ cache is generally built from SRAM.
c) In two-level caches the $L_1$ cache is generally larger than $L_2$ cache.
d) In two-level caches, the $L_2$ cache generally has a lower latency than the $L_1$ cache.

Common Data questions Q13 and Q14

Consider an accumulator-based CPU which supports only single address instruction. The CPU supports the following instructions.
LOAD A - Load A from memory into the accumulator AC.
STORE A - Store contents of accumulator AC in memory location M.
ADD B - Load B into data register (DR) and add to accumulator.
MOVE A, B - Move content of B to A.
SUB A, B - Subtract B from A.

Q13. Assume CPU uses the memory referencing and each instruction LOAD, STORE and ADD takes one clock cycle. To compute Z = X + Y CPU takes how many minimum number of clock cycles ?

a) 2
b) 3
c) 4
d) 5

Q14. How many minimum clock cycles are needed when accumulator becomes 0. If each instruction takes one clock cycle ?

a) 0
b) 1
c) 2
d) 3

Common Data Questions for 15 and 16.

Assume a fully associative write-back cache with many cache entries that start empty. We define a sequence of memory operations. The address or locations is in square brackets.

$S_1$ : Write M[100];
$S_2$ : Write M[100];
$S_3$ : Read M[200];
$S_4$ : Write M[200];

$S_5$ : Write M[100];

Q15. What are the number of hits when using no write allocate versus write allocate ?

a) 2, 1
b) 2, 2
c) 1, 3
d) 4, 1

Q16. What are the number of misses when using no write allocate versus write allocate ?

a) 2, 1
b) 2, 4
c) 3, 3
d) 4, 2

Common data questions for 17 and 18.

Suppose a CPU contains 1000 memory references there are 40 misses in $L_1$ cache (First level Cache) and 20 misses in the $L_2$ cache (Second level cache). Assume miss penalty from the $L_2$ cache to memory is 100 clock cycles, the hit time of $L_2$ cache is 10 clock cycles, the hit time of $L_1$ cache is 1 clock cycle and there are 1.5 memory references per instruction.

Q17. What is the average memory access time ?

a) 3.4 clock cycles
b) 3.5 clock cycles
c) 5.3 clock cycles
d) 1.8 clock cycles

Q18. What is the average memory stalls per instruction ?

a) 3.4 clock cycles
b) 3.5 clock cycles
c) 3.6 clock cycles
d) 4.5 clock cycles

Q19. A 2-level memory has an average access time of 30 ns with cache and memory access time as 20 ns and 150 ns respectively. What is the hit ratio ?

a) 80%
b) 93%
c) 70%
d) 99%

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Q20. Consider the unpipelined machine with 10 ns clock cycles. It uses four cycles for ALU operations and branches, whereas five cycles for memory operations. Assume that the relative frequencies of their operations are 40%, 20% and 40% respectively. Suppose that due to clock skep and setup, pipelining the machine adds 1 ns overhead to the clock. How much speed up in the instruction execution rate will we gain from a pipeline ?

a) 5 times
b) 8 times
c) 4 times
d) 4.5 times

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Answer Key :-

1. B
2. B
3. B
4. D
5. D
6. D
7. D
8. D
9. D
10. B
11. C
12. B
13. B
14. D
15. C
16. D
17. A
18. C
19. B
20. C